IN THE SPECIFICATION:

Paragraph beginning at line 2 of page 8 has been amended as follows:

Embodiments of the present invention will be described below with reference to the accompanying drawings. Fig. 1 is a schematic sectional view of an N-channel vertical MOS transistor according to the present invention. A semiconductor substrate shown in Fig. 1 is prepared by forming, through epitaxial growth, on a heavily doped substrate 1 of a first conductivity type which serves as a drain region, a first conductivity type layer 2 doped with an impurity that is used to dope the substrate 1 in a concentration lower than that of the substrate 1. A surface of the thus prepared semiconductor substrate is subjected to impurity implantation and subsequent high temperature heat treatment at 1,000°C or more to form a diffusion region 3 of a second conductivity type, which serves, as a body region. The other portions of the surface of the substrate constitute a high concentration impurity region 7 of the first conductivity type which serves as a source region and a heavily doped body contact region 8 of the second conductivity type which fixes an electric potential of the body region by ohmic contact. The regions 7 and 8 are turned conductive by the same metal

film. As a contact between the regions 7 and 8, a silicon surface is uniformly exposed except in a silicon trench 4 to bring the metal film into contact with the semiconductor substrate flatly.

Paragraph beginning at line 7 of page 9 has been amended as follows:

The heavily doped polycrystalline silicon gate electrode 6 in the trench 4 is desirably 0.5 μm or deeper from the top of the trench. This is for preventing a capacitor that is formed between the gate electrode and a source metal electrode 15 immediately above the gate electrode from impairing high frequency characteristics. Considering the diffusion depth of the heavily doped source region, it is desirable to set the heavily doped polycrystalline silicon gate electrode 6 to 1 μm or shallower from the top of the trench 4. If the source region is ~~let diffuse~~ allowed to be diffused deeper than that through heat treatment, the depth of the body region is accordingly changed.

Paragraph beginning at line 17 of page 9 has been amended as follows:

In short, the heavily doped polycrystalline silicon gate electrode 6 is preferably set between 0.5 μm and 1 μm down from the top of the trench 4.

Paragraph beginning at line 2 of page 10 has been amended as follows:

First, a <100> orientation semiconductor substrate is prepared by forming an N type lightly doped <u>epitaxial growth layer or</u> epitaxial layer 2 to a thickness of several μm to several tens μm on an N type heavily doped substrate 1 (Fig. 3). The N type heavily doped substrate 1 is doped with As or SB in a concentration that gives the substrate a resistivity of 0.001 $\Omega\cdot$cm to 0.01 $\Omega\cdot$cm. The N type lightly doped epitaxial layer 2 is doped with P in a concentration of 2e14/cm^3 to 4e16/cm^3. The thickness and impurity concentration of the N type epitaxial layer are arbitrarily set in accordance with the necessary drain-source withstand voltage and current drive performance.

Paragraph beginning at line 12 of page 11 has been amended as follows:

Next, a region to later serve as a body of the vertical MOS transistor is formed by subjecting the semiconductor substrate to implantation of B and subsequently to heat treatment. Obtained as a result is a P type body region 3 having an impurity concentration of 2e16/cm^3 to 5e16/cm^3 and a thickness of several μm to over ten μm. Then single crystal silicon is exposed in a region where a trench

is to be formed while the rest is covered with an oxide film mask or a resist mask in preparation for anisotropic etching by RIE. The exposed silicon is etched until the body region is pierced and a silicon trench is thus formed. <u>More specifically, the silicon trench 4 is formed so that it pierces the body region 3 until it reaches an inner part of the epitaxial layer 2.</u>

Paragraph beginning at line 22 of page 11 has been amended as follows:

Corners of the trench are rounded by a well known method such as high temperature sacrificial oxidation or isotropic dry etching. Then a gate insulating film <u>5</u> is formed on the side walls and bottom <u>(i.e., side wall surfaces and bottom surfaces)</u> of the trench <u>4</u> (Fig. 4).

Paragraph beginning at line 20 of page 13 has been amended as follows:

Formed next is a metal film 15 for giving the source and body electric potentials (Fig. 10). Unlike conventional cases in which the heavily doped source region and the heavily doped body region alone are selectively brought into contact with the metal film by forming a contact hole in the intermediate insulating film, the present invention can

establish a metal contact while the metal film is formed on the entire transistor region since the heavily doped polycrystalline silicon 6 in the trench is covered with the intermediate insulating film. In addition, the metal film is highly flat (i.e., generally planar) due to the fact that the substrate surface on which the metal film is formed is previously leveled by etch-back.

Paragraph beginning at line 6 of page 15 has been amended as follows:

Fig. 12 shows another embodiment of the present invention. In Fig. 12, an insulator in the form of side spacers 18 are formed from a nitride film or the like on the side walls of the trench 4 above the heavily doped polycrystalline silicon 6. In general, electric field concentration tends to take place in an oxide film between heavily doped polycrystalline silicon and a heavily doped source region in a vertical MOS transistor, and the oxide film in this portion is liable to undergo film quality degradation due to etching or other damage brought upon in the manufacturing process. These are two factors that readily cause lowering of the oxide film withstand voltage, lowering of the long-term reliability, and other defects. The present

invention is capable of avoiding such defects by forming a nitride film in this portion in this embodiment as shown in Fig. 12.

Paragraph beginning at line 20 of page 15 has been amended as follows:

The side spacers 18 can be formed by depositing a nitride and subjecting the deposit to anisotropic dry etching in the step of Fig. 7, which shows a part of the manufacturing process of the present invention.